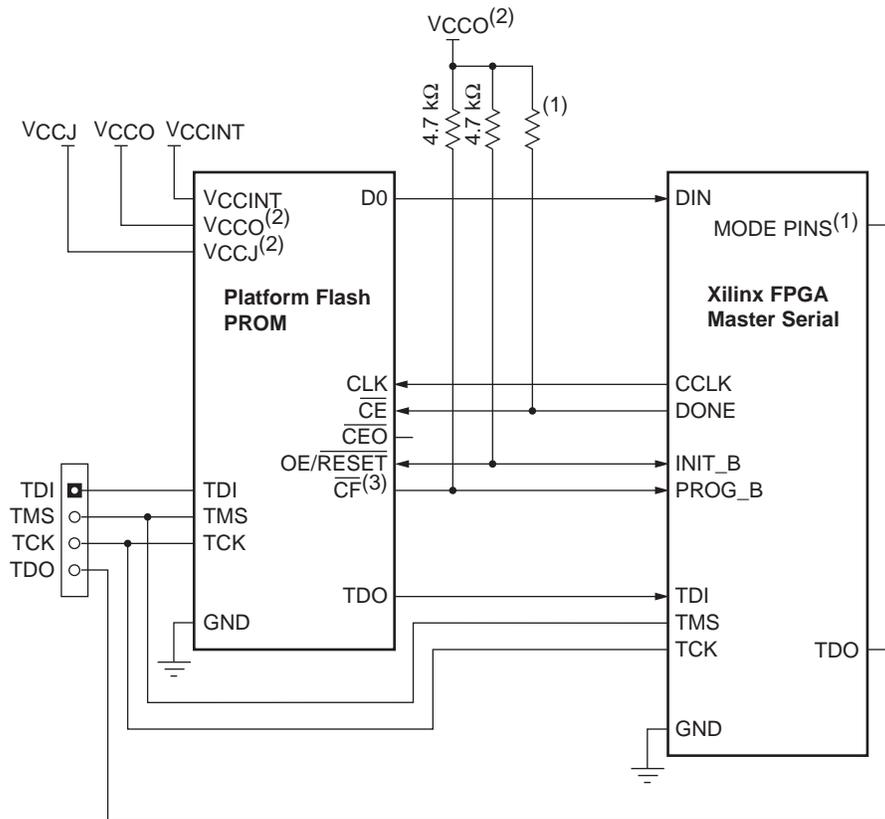


Configuring in FPGA Master Serial Mode

Master Serial configuration mode (shown in Figure 2-1) is most commonly used with configuration PROMs, because it is simple to implement. Only a small number of signals are required to interface the PROM with the FPGA, and an external clock source is not required for configuration. In FPGA Master Serial mode, the FPGA generates the configuration clock. In this mode, data is available on the PROM Data (D0) pin when \overline{CF} is High, and \overline{CE} and OE are enabled. New data is available a short access time after each rising clock edge.



Notes:

- 1 For Mode pin connections and DONE pin pull-up value, refer to the appropriate FPGA data sheet.
- 2 For compatible voltages, refer to the appropriate data sheet.
- 3 For XCFxxS devices, the \overline{CF} pin is an output pin. For XCFxxP devices, the \overline{CF} pin is a bidirectional pin.

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Figure 2-1: FPGA Master Serial Configuration Setup

Choose a Configuration Mode: M[2:0]

The mode select pins, M[2:0], define the configuration mode that the FPGA uses to load its bitstream, as shown in [Table 2-1](#). The logic levels applied to the mode pins is sampled on the rising edge of [INIT_B](#), immediately after the FPGA completes initializing its internal configuration memory.

Table 2-1: Mode Pin Settings and Associated FPGA Configuration Mode by Family

M[2:0]	FPGA Family			
	Spartan-3	Spartan-3E	Spartan-3A Spartan-3A DSP	Spartan-3AN
<0:0:0>	Master Serial (Platform Flash) Mode			
<0:0:1>	Reserved	Master SPI Mode		
<0:1:0>	Reserved	BPI Up		
<0:1:1>	Master Parallel	BPI Down	Reserved	Internal Master SPI
<1:0:0>	Reserved			
<1:0:1>	JTAG Mode			
<1:1:0>	Slave Parallel Mode			
<1:1:1>	Slave Serial Mode			

M[2:0] Functional Differences between Spartan-3 Generation Families

[Table 2-2](#) summarizes the slight differences in functionality between the Spartan-3 generation families.

Table 2-2: M[2:0] Mode Pin Differences between Spartan-3 Generation FPGAs

	Spartan-3 FPGA	Spartan-3E FPGA	Extended Spartan-3A Family FPGAs
Available as possible user I/O pin after configuration?	No	Yes	Yes
Dedicated internal pull-up resistor during configuration?	Yes	No	Yes
Mechanism to define post-configuration behavior	<i>M2Pin</i> , <i>M1Pin</i> , <i>M0Pin</i> bitstream options	User I/O	User I/O
Input supply voltage	V _{CCAUX}	V _{CCO_2}	V _{CCO_2}
Output supply voltage	N/A	V _{CCO_2}	V _{CCO_2}
Same voltage as other pins in the configuration interface?	Only when interface is at 2.5V	Yes	Yes

Program or Reset FPGA: PROG_B

The PROG_B pin is an asynchronous control input to the FPGA. When Low, the PROG_B pin resets the FPGA, initializing the configuration memory. When released, the PROG_B begins the configuration processes. The initialization process does not start until PROG_B returns High. Asserting PROG_B Low for an extended period delays the configuration process. The various PROG_B functions are outlined in [Table 2-7](#).

At power-up or after a master reset, PROG_B always has a pull-up resistor to V_{CCAUX} , regardless of the “[Pull-Up Resistors During Configuration](#)” control input. After configuration, the bitstream generator option *ProgPin* defines whether or not the pull-up resistor is remains active. By default, the *ProgPin* option retains the pull-up resistor.

Table 2-7: **PROG_B Operation**

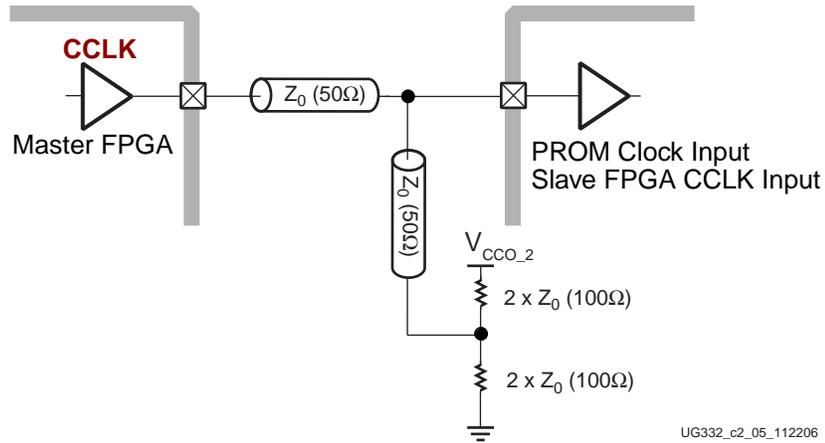
PROG_B Input	Response
Power-up	Internal “ Power-On Reset (POR) ” circuit automatically initiates FPGA configuration process.
Low-going pulse 	Initiate (re)configuration process and continue to completion.
Extended Low 	Initiate (re)configuration process and stall process in the “ Clear Configuration Memory (Initialization) ” step. Configuration is stalled until PROG_B returns High.
1	If the configuration process is started, continue to completion. If configuration process is complete, the FPGA remains configured.

After configuration, hold the PROG_B input High. Any Low-going pulse on PROG_B, lasting 500 ns or longer (300 ns in the Spartan-3 FPGAs), restarts the configuration process.

The PROG_B pin functionality is identical among all Spartan-3 generation FPGAs.

Figure 2-3 shows the basic point-to-point topology where the CCLK output from the Master FPGA drives one clock input receiver, either on the configuration PROM or on a slave FPGA.

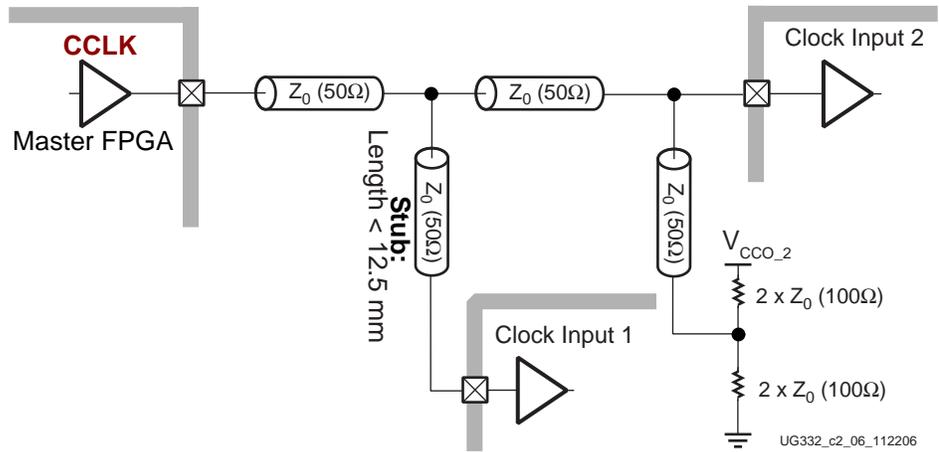
Caution! On Spartan-3E and Extended Spartan-3A family FPGAs, be sure to define a valid logic level on CCLK. Otherwise, the clock trace might float and cause spurious clocking to other devices in the system.



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Figure 2-3: Point-to-Point: Master CCLK Output Drives Single Clock Load

Figure 2-4 shows the basic multi-drop flyby topology where the CCLK output from the Master FPGA drives two or more clock input receivers. Constrain the trace length on any clock stubs.



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Figure 2-4: Multi-Drop: Master CCLK Output Drives Two Clock Inputs

Figure 2-5 shows a star topology where the Master FPGA CCLK transmission line branches to the multiple clock receiver inputs. The branch point creates a significant impedance discontinuity. Do not use this topology.

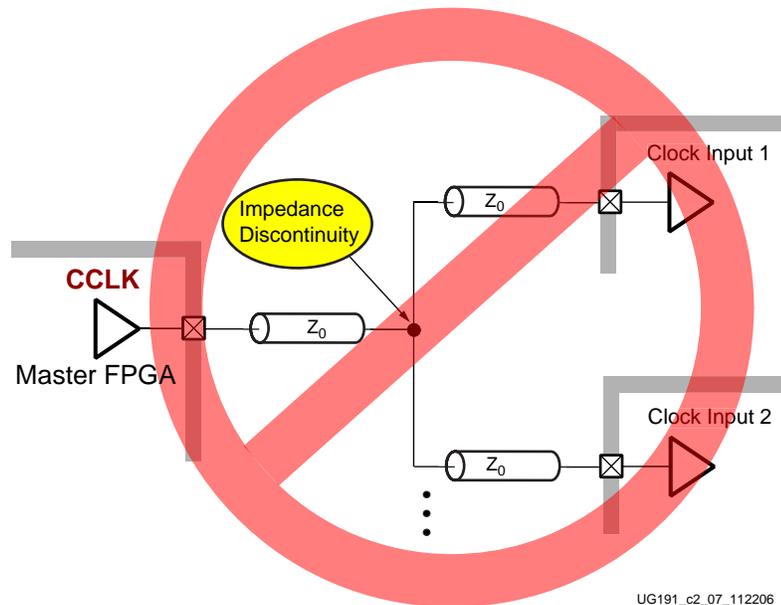


Figure 2-5: Star Topology Is Not Recommended

ConfigRate: Bitstream Option for CCLK

For Master configuration mode, the *ConfigRate* bitstream generator option defines the frequency of the internally-generated CCLK oscillator. The actual frequency is approximate due to the characteristics of the silicon oscillator and varies by up to 50% over the temperature and voltage range. On Spartan-3E and Extended Spartan-3A family FPGAs, the resulting frequency for every *ConfigRate* setting is fully characterized and specified in the associated FPGA family data sheet. At power-on, CCLK always starts operation at its lowest frequency. Use the *ConfigRate* option to set the oscillator frequency to one of the other values shown in Table 2-8.

Set this option graphically in “ISE Software Project Navigator,” page 42, as shown in Step 7 in Figure 1-7, page 44.

The FPGA does not start operating at the higher CCLK frequency until the *ConfigRate* control bits are loaded during the configuration process.

Persist: Reserve CCLK As Part of SelectMAP Interface

By default, any clocks applied to CCLK after configuration are ignored unless the bitstream option *Persist:Yes* is set, which retains the configuration interface. If *Persist:Yes*, then all clock edges are potentially active events, depending on the other configuration control signals. On Spartan-3E and Extended Spartan-3A family FPGAs, CCLK becomes a full-featured user-I/O pin after configuration.

Table 2-9: Pins with Dedicated Pull-Up Resistors during Configuration (All Spartan-3 Generation FPGAs)

Pin Name	Pull-Up Resistor Supply Rail	Post Configuration Control
PROG_B	V _{CCAUX}	<i>ProgPin</i> BitGen setting
DONE	V _{CCAUX}	<i>DonePin</i> and <i>DriveDone</i> BitGen settings
Pull-up during Configuration control input, HSWAP, PUDC_B, or HSWAP_EN (see Table 2-12)	V _{CCO_0}	<i>Spartan-3E and Extended Spartan-3A family FPGAs</i> : User I/O after configuration. Controlled by the FPGA application <i>Spartan-3 FPGA</i> : Controlled by <i>HswapenPin</i> BitGen setting
INIT_B	<i>Spartan-3E/3A/3AN/ Spartan-3A DSP FPGAs</i> : V _{CCO_2} <i>Spartan-3 FPGA</i> : V _{CCO_4} or V _{CCO_BOTTOM}	User I/O after configuration. Controlled by the FPGA application
TDI	V _{CCAUX}	<i>TdiPin</i> BitGen setting
TMS	V _{CCAUX}	<i>TmsPin</i> BitGen setting
TCK	V _{CCAUX}	<i>TckPin</i> BitGen setting
TDO	V _{CCAUX}	<i>TdoPin</i> BitGen setting

As highlighted in Table 2-2, page 50, the Extended Spartan-3A family FPGAs add a few more dedicated internal pull-up resistors, as shown in Table 2-10. On Spartan-3E FPGAs, these pins do not have a dedicated internal pull-up resistor, but do have an optional pull-up resistor controlled when HSWAP = 0.

Table 2-10: Pins with Dedicated Pull-Up Resistors during Configuration (Extended Spartan-3A Family FPGAs Only)

Pin Name	Pull-Up Resistor Supply Rail	Post Configuration Control
M[2:0]	V _{CCO_2}	User I/O after configuration. Controlled by the FPGA application
VS[2:0]	V _{CCO_2}	Pull-up resistors only active when M[2:0]=<0:0:1>, Master SPI mode, or in Spartan-3AN FPGAs when M[2:0]=<0:1:1>, Internal Master SPI mode. User I/O after configuration. Controlled by the FPGA application

The Spartan-3 FPGA family uses dedicated configuration pins, as shown in Table 2-11. The post-configuration behavior is controlled by bitstream settings.

Table 2-13: Pull-Up Resistor Ranges by Spartan-3 Generation Family

Voltage Range	Spartan-3 FPGA	Spartan-3E FPGA	Spartan-3A/3AN Spartan-3A DSP FPGA	Units
V_{CCAUX} or $V_{CCO} = 3.0$ to $3.6V$			5.1 to 23.9	k Ω
$V_{CCO} = 3.0$ to $3.45V$	1.27 to 4.11	2.4 to 10.8		
V_{CCAUX} or $V_{CCO} = 2.3$ to $2.7V$	1.15 to 3.25	2.7 to 11.8	6.2 to 33.1	
$V_{CCO} = 1.7$ to $1.9V$	2.45 to 9.10	4.3 to 20.2	8.4 to 52.6	

Table 2-14: Recommended External Pull-Up or Pull-down Resistor Values to Define Input Values during Configuration

PUDC_B, HSWAP, or HSWAP_EN	Desired Pull Direction	I/O Standard	Spartan-3 FPGA	Spartan-3E FPGA	Spartan-3A/3AN Spartan-3A DSP FPGA
= 0 (also applies to all pins that have a dedicated pull-up resistor during configuration, see “Pins with Dedicated Pull-Up Resistors during Configuration,” page 62)	Pull-Up	All	No pull-up required. Internal pull-up resistors are enabled. See Table 2-13 for resistor range.		
	Pull-Down (required to overcome maximum I_{RPU} current and guarantee V_{IL})	LVC MOS33 LV TTL	$\leq 330 \Omega$	$\leq 620 \Omega$	$\leq 1.1 \text{ k}\Omega$
		LVC MOS25	$\leq 470 \Omega$	$\leq 820 \Omega$	$\leq 1.8 \text{ k}\Omega$
		LVC MOS18	$\leq 510 \Omega$	$\leq 820 \Omega$	$\leq 3.3 \text{ k}\Omega$
		LVC MOS15	$\leq 820 \Omega$	$\leq 1.2 \text{ k}\Omega$	$\leq 5.4 \text{ k}\Omega$
LVC MOS12	$\leq 1.5 \text{ k}\Omega$	$\leq 1.5 \text{ k}\Omega$	$\leq 9.6 \text{ k}\Omega$		
= 1 (optional pull-up resistors are disabled during configuration. Does not apply to pins with dedicated pull-up resistors during configuration)	Pull-Up (required to overcome single-load, maximum I_L leakage current and guarantee V_{IH})	LVC MOS33 LV TTL	$\leq 40 \text{ k}\Omega$	$\leq 100 \text{ k}\Omega$	
		LVC MOS25	$\leq 60 \text{ k}\Omega$		
		LVC MOS18	$\leq 37 \text{ k}\Omega$		
		LVC MOS15	$\leq 28 \text{ k}\Omega$		
		LVC MOS12	$\leq 38 \text{ k}\Omega$		
	Pull-Down (required to overcome single-load, maximum I_L leakage current and guarantee V_{IL})	LVC MOS33 LV TTL	$\leq 32 \text{ k}\Omega$	$\leq 80 \text{ k}\Omega$	
		LVC MOS25	$\leq 70 \text{ k}\Omega$		
		LVC MOS18	$\leq 38 \text{ k}\Omega$		
		LVC MOS15			
		LVC MOS12	$\leq 59 \text{ k}\Omega$		

Pin Descriptions

Table 2-15 lists the various pins involved in the configuration process, including which configuration mode, the pin’s direction, and a summary description. The table also describes how to use the pin during and after configuration.

Table 2-15: Spartan-3 Generation Configuration Pins, Associated Modes, and Function

Pin Name	Config. Mode(s)	FPGA Direction	Description	During Configuration	After Configuration
HSWAP or PUDC_B or HSWAP_EN (depends on FPGA family)	All	Input	User I/O Pull-Up Control. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V _{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	Spartan-3: Dedicated pin (don't care after configuration) Spartan-3E Spartan-3A Spartan-3AN Spartan-3A DSP: User I/O
M[2:0]	All	Input	Mode Select. Selects the FPGA configuration mode as defined in Table 2-1 .	Must be at the logic levels shown in Table 2-1, page 50 . Sampled when INIT_B goes High.	User I/O (dedicated on Spartan-3 FPGAs)
DIN	Serial Modes, SPI	Input	Serial Data Input. for all serial configuration modes	Receives serial data from PROM serial data output.	User I/O
CCLK	Master Modes, SPI, BPI	Output (treat as I/O for signal integrity)	Configuration Clock. Generated by FPGA internal oscillator. Frequency controlled by ConfigRate bitstream generator option. See "Configuration Clock: CCLK," page 56 .	Drives PROM's clock input.	User I/O (dedicated on Spartan-3 FPGAs)
	Slave Modes	Input	Configuration clock input.	Input configuration clock source.	
DOUT		Output	Serial Data Output.	Not used in single-FPGA designs; DOUT is pulled up, not actively driving. In a serial daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	All	Open-drain bidirectional I/O	Initialization Indicator. Active Low. See "Initializing Configuration Memory, Configuration Error: INIT_B," page 61 .	Drives Low after power-on reset (POR) or when PROG_B pulsed Low while the FPGA is clearing its configuration memory. If a CRC error detected during configuration, FPGA again drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High or Low to avoid a floating value. See INIT_B "After Configuration".

Table 2-15: Spartan-3 Generation Configuration Pins, Associated Modes, and Function (Cont'd)

Pin Name	Config. Mode(s)	FPGA Direction	Description	During Configuration	After Configuration
DONE	All	Open-drain bidirectional I/O	FPGA Configuration Done. Low during configuration. Goes High when FPGA successfully completes configuration. Powered by V_{CCAUX} supply. 0: FPGA not configured 1: FPGA configured See “DONE Pin,” page 52	Actively drives Low during configuration.	When High, indicates that the FPGA successfully configured.
PROG_B	All	Input	Program FPGA. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins. If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor. See “Program or Reset FPGA: PROG_B ,” page 56.	Must be High during configuration to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.
Spartan-3E Spartan-3A Spartan-3AN Spartan-3A DSP FPGA: VS[2:0]	Master SPI	Input	Variant Select. Instructs the FPGA how to communicate with the attached SPI Flash PROM.	Must be at the logic levels shown in Table 4-2, page 105 . Sampled when INIT_B goes High.	User I/O
Spartan-3E Spartan-3A Spartan-3AN Spartan-3A DSP FPGA: MOSI	Master SPI	Output	Serial Data Output.	FPGA sends SPI Flash memory read commands and starting address to the PROM’s serial data input.	User I/O
Spartan-3E Spartan-3A Spartan-3AN Spartan-3A DSP FPGA:CSO_B	Master SPI	Output	Chip Select Output. Active Low.	Connects to the SPI Flash PROM’s Slave Select input. If $HSWAP/PUDC_B = 1$, connect this signal to a 4.7 k Ω pull-up resistor to 3.3V.	Drive CSO_B High after configuration to disable the SPI Flash and reclaim the MOSI , DIN , and CCLK pins. Optionally, re-use this pin and MOSI , DIN , and CCLK to continue communicating with SPI Flash.

Table 2-15: Spartan-3 Generation Configuration Pins, Associated Modes, and Function (Cont'd)

Pin Name	Config. Mode(s)	FPGA Direction	Description	During Configuration	After Configuration
Spartan-3E Spartan-3A Spartan-3AN Spartan-3A DSP FPGA: CSL_B Spartan-3 FPGA: CS_B	BPI, Slave Parallel	Input	Chip Select Input. Active Low.	Active-Low.	User I/O. If bitstream option <i>Persist:Yes</i> , becomes part of SelectMap parallel peripheral interface.
RDWR_B	BPI, Slave Parallel	Input	Read/Write Control. Active Low write enable. Read functionality typically only used after configuration, if bitstream option <i>Persist:Yes</i> .	Must be Low throughout configuration. Do not change logic level while <i>CSL_B</i> is Low	User I/O. If bitstream option <i>Persist:Yes</i> , becomes part of SelectMap parallel peripheral interface.
Spartan-3E Spartan-3A Spartan-3AN Spartan-3A DSP FPGA: LDC0	BPI	Output	PROM Chip Enable	Connect to parallel PROM chip-select input (<i>CS#</i>). FPGA drives this signal Low throughout configuration.	User I/O. If the FPGA does not access the PROM after configuration, drive this pin High to deselect the PROM. A[23:0], D[7:0], LDC[2:1], and HDC then become available as user I/O.
Spartan-3E Spartan-3A Spartan-3AN Spartan-3A DSP FPGA: LDC1	BPI	Output	PROM Output Enable	Connect to the parallel PROM output-enable input (<i>OE#</i>). The FPGA drives this signal Low throughout configuration.	User I/O
Spartan-3E Spartan-3A Spartan-3AN Spartan-3A DSP FPGA: HDC	BPI	Output	PROM Write Enable	Connect to parallel PROM write-enable input (<i>WE#</i>). FPGA drives this signal High throughout configuration.	User I/O
Spartan-3E Spartan-3A Spartan-3AN Spartan-3A DSP FPGA: LDC2	BPI	Output	PROM Byte Mode	This signal is not used for x8 PROMs. For PROMs with a x8/x16 data width control, connect to PROM byte-mode input (<i>BYTE#</i>).	User I/O. Drive this pin High after configuration to use a x8/x16 PROM in x16 mode.

Table 2-15: Spartan-3 Generation Configuration Pins, Associated Modes, and Function (Cont'd)

Pin Name	Config. Mode(s)	FPGA Direction	Description	During Configuration	After Configuration
Spartan-3E FPGA: A[23:0] Spartan-3A Spartan-3AN Spartan-3A DSP FPGA: A[25:0]	BPI	Output	Parallel PROM Address outputs	Connect to PROM address inputs.	User I/O.
D[7:0]	Master Parallel, BPI, Slave Parallel, SelectMAP	Input	Data Input	Data captured by FPGA	User I/O. If bitstream option <i>Persist:Yes</i> , becomes part of SelectMap parallel peripheral interface.
Spartan-3/ Spartan-3E FPGA: BUSY	BPI, Slave Parallel (SelectMAP)	Output	FPGA Busy Indicator. Used primarily in Slave Parallel interfaces that operate at 50 MHz and faster. Same function is on DOUT pin in the Extended Spartan-3A family.	Not used during BPI mode configuration but actively drives.	User I/O. If bitstream option <i>Persist:Yes</i> , becomes part of SelectMap parallel peripheral interface.

Pin Behavior During Configuration

Table 2-16, Table 2-17, and Table 2-18 show how various pins on Spartan-3 generation FPGAs behave during the configuration process. The actual behavior depends on the settings applied to the M2, M1, and M0 (M[2:0]) mode select pins and the pin that controls the optional pull-up resistors, called HSWAP, PUDC_B, or HSWAP_EN depending on the specific Spartan-3 generation FPGA family. The M[2:0] mode select pins determine which of the I/O pins are active and borrowed during configuration and how they function. In JTAG configuration mode, no user-I/O pins are borrowed for configuration.

The **Dedicated Pull-Up Resistor** column indicates pins that always have a pull-up resistor enabled during configuration, regardless of the PUDC_B, HSWAP, or HSWAP_EN input. After configuration, the behavior of these pins is either defined by specific bitstream generator options or by the FPGA application itself.

Table 2-16, Table 2-17, and Table 2-18 show the FPGA pins that are either borrowed or dedicated during configuration. The specific pins are listed by FPGA configuration mode along the top. For each pin, the table also indicates the power rail that supplies the pin during configuration. A numeric value such as “2”, indicates that the associated pin is located in I/O Bank 2 and powered by the VCCO_2 supply inputs. Spartan-3E and Extended Spartan-3A family FPGAs have four I/O banks; the Spartan-3 FPGA family has eight I/O banks.

The pin names are color-coded using the same colors used in the package pinout tables and footprint diagrams found in the respective Spartan-3 generation data sheet. Black represents the dedicated JTAG pins; yellow represents the dedicated configuration pins; light blue represents the dual-purpose configuration pins that become user-I/O pins after configuration.

Supported Platform Flash PROMs

Table 3-4 shows the smallest available Platform Flash PROM to program one Spartan-3 generation FPGA. A multiple-FPGA daisy-chain application requires a Platform Flash PROM large enough to contain the sum of the various FPGA bitstream sizes.

Table 3-4: Number of Bits to Program a Spartan-3 Generation FPGA and Smallest Platform Flash PROM

Family	FPGA	Number of Configuration Bits	Smallest Possible Platform Flash PROM
Spartan-3A (Spartan-3AN)	XC3S50A	437,312	XCF01S
	XC3S200A	1,196,128	XCF02S
	XC3S400A	1,886,560	XCF02S
	XC3S700A	2,732,640	XCF04S
	XC3S1400A	4,755,296	XCF08P or XCF04S + XCF02S
Spartan-3A DSP	XC3SD1800A	8,197,280	XCF08P or two XCF04S PROMs
	XC3SD3400A	11,718,304	XCF16P
Spartan-3E	XC3S100E	581,344	XCF01S
	XC3S250E	1,353,728	XCF02S
	XC3S500E	2,270,208	XCF04S
	XC3S1200E	3,841,184	XCF04S
	XC3S1600E	5,969,696	XCF08P or XCF04S + XCF02S
Spartan-3	XC3S50	439,264	XCF01S
	XC3S200	1,047,616	XCF01S
	XC3S400	1,699,136	XCF02S
	XC3S1000	3,223,488	XCF04S
	XC3S1500	5,214,784	XCF08P or XCF04S + XCF02S
	XC3S2000	7,673,024	XCF08P or 2 x XCF04S
	XC3S4000	11,316,864	XCF16P
	XC3S5000	13,271,936	XCF16P

There are two possible design solutions for FPGA designs that require 8 Mbit PROMs: use either a single 8 Mbit XCF08P parallel/serial PROM or two cascaded XCFxxS serial