OPA855, 8 GHz Gain Bandwidth Product, Gain of 7 V/V Stable, Bipolar Input Amplifier

1 Features

- High Gain Bandwidth Product: 8 GHz
- Decompensated, Gain ≥ 7 V/V (Stable)
- Low Input Voltage Noise: 0.98 nV/√Hz
- Slew Rate: 2750 V/µs
- Low Input Capacitance:
  - Common-Mode: 0.6 pF
  - Differential: 0.2 pF
- Wide Input Common-Mode Range:
  - 0.4 V from Positive Supply
  - 1.1 V from Negative Supply
- 3 V_{PP} Output Swing in TIA Configuration
- Supply Voltage Range: 3.3 V to 5.25 V
- Quiescent Current: 17.5 mA
- Available in 8-Pin WSON Package
- Temperature Range: –40 to +125°C

2 Applications

- High-Speed Transimpedance Amplifier
- Laser Distance Measurement
- Lidar Receivers
- Level Transmitter (Optical)
- Optical Time Domain Reflectometry (OTDR)
- Distributed Temperature Sensing
- 3D Scanner
- Time-of-Flight (ToF) Systems
- Autonomous Driving Systems

3 Description

The OPA855 is a wideband, low-noise, operational amplifier with bipolar inputs for wideband transimpedance and voltage amplifier applications. When the device is configured as a transimpedance amplifier (TIA), the 8-GHz gain bandwidth product (GBWP) enables applications requiring high closed-loop bandwidths at transimpedance gains up to tens of kΩs.

The OPA855 device is available in a 2-mm × 2-mm, 8-pin, WSON package. The package features a feedback pin (FB) that simplifies the feedback network connection between the input and the output. There is a no-connect (NC) pin between the FB pin and the inverting input (IN–) of the amplifier that increases the physical spacing between the FB and IN– pins thereby decreasing the parasitic capacitive coupling between them. Minimizing parasitic capacitance on the amplifiers input and output node is crucial to maximizing signal integrity in photodiode and Lidar applications.

The OPA855 has been optimized for use in optical Time-of-Flight (ToF) systems like the one shown in the figure below where the OPA855 is used in conjunction with the TDC7201, time to digital converter. The OPA855 may also be used in high-resolution Lidar systems with a high-speed Analog-to-Digital converter (ADC) and a differential output amplifier like the THS4541 or LMH5401 to drive the ADC.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA855	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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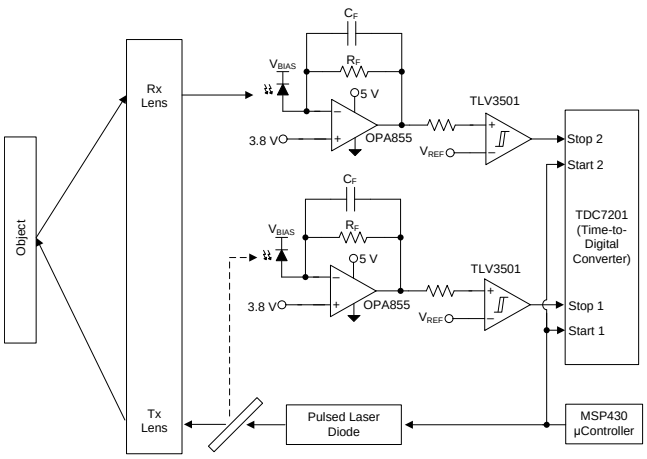
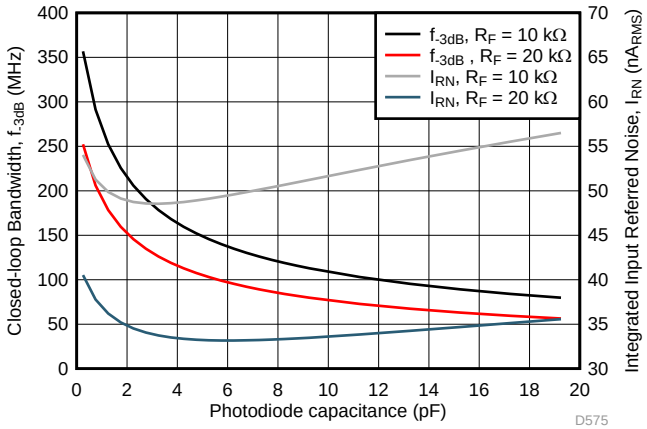
High-Speed Time-of-Flight Receiver



Photodiode Capacitance vs. Bandwidth and Noise



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

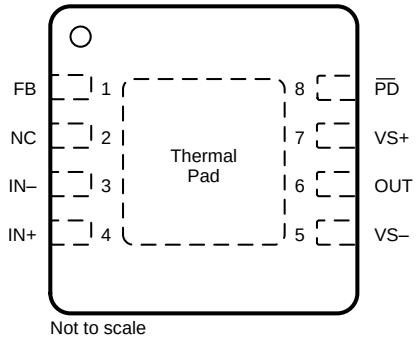
DATE	REVISION	NOTES
July 2018	*	Initial release.

5 Device Comparison Table

DEVICE	INPUT TYPE	MINIMUM STABLE GAIN	GAIN BANDWIDTH
OPA855	BJT	7 V/V	8 GHz
OPA858	CMOS	7 V/V	5.5 GHz

6 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

NC - no internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	1	I	Feedback connection to output of amplifier
IN–	3	I	Inverting input
IN+	4	I	Noninverting input
NC	2	—	Do not connect
OUT	6	O	Amplifier output
$\overline{PD}$	8	I	Power down connection. $\overline{PD}$ = logic low = power off mode; $\overline{PD}$ = logic high = normal operation
VS–	5	—	Negative voltage supply
VS+	7	—	Positive voltage supply
Thermal pad		—	Connect the thermal pad to VS–

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)		5.5	V
V_{IN+}, $V_{IN–}$	Input voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	
V_{ID}	Differential input voltage		1	
V_{OUT}	Output voltage	($V_{S–}$) – 0.5	(V_{S+}) + 0.5	
I_{IN}	Continuous input current		±10	mA
I_{OUT}	Continuous output current(2)		±100	
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature		125	
T_{STG}	Storage temperature	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Long-term continuous output current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage (V_{S+} – $V_{S–}$)	3.3	5	5.25	V

7.4 Thermal Information

THERMAL METRIC(1)		OPA855 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	100	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	22.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

V_{S+} = 5 V, $V_{S–}$ = 0 V, G = 7 V/V, R_F = 453 Ω, noninverting configuration, input common-mode biased at midsupply, R_L = 200 Ω, output load is referenced to midsupply, and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_{OUT} = 200 mV_{PP}		2.5		GHz	C
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		850		MHz	C
GBP	Gain-bandwidth product			8		GHz	C
	Bandwdith for 0.1-dB flatness			200		MHz	C
SR	Slew rate (10%-90%)	V_{OUT} = 2-V step		2750		V/µs	C
t_r	Rise time	V_{OUT} = 200-mV step		0.17		ns	C
t_f	Fall time	V_{OUT} = 200-mV step		0.17		ns	C
	Settling time to 0.1%	V_{OUT} = 2-V step		8		ns	C
	Settling time to 0.001%	V_{OUT} = 2-V step		3000		ns	C
	Overshoot or undershoot	V_{OUT} = 2-V step		7%			C
	Overdrive recovery	2x output overdrive		3		ns	C
HD2	Second-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		80		dBc	C
		f = 100 MHz, V_{OUT} = 2 V_{PP}		59			
HD3	Third-order harmonic distortion	f = 10 MHz, V_{OUT} = 2 V_{PP}		86		dBc	C
		f = 100 MHz, V_{OUT} = 2 V_{PP}		63			
e_n	Input-referred voltage noise	f = 1 MHz		0.98		nV/rHz	C
e_i	Input-referred current noise	f = 1 MHz		2.3		pA/rHz	C
z_O	Closed-loop output impedance	f = 100 kHz		0.1		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain		70	75		dB	A
V_{OS}	Input offset voltage	T_A = 25°C	–2.5	0.05	2.5	mV	A
$\Delta V_{OS}/\Delta T$	Input offset voltage drift	T_A = –40°C to +85°C		1.25		µV/°C	B
I_B	Input bias current (1)	T_A = 25°C	–5	–12	–18.5	µA	A
$\Delta I_B/\Delta T$	Input bias current drift	T_A = –40°C to +85°C		0.3		µA/°C	B
I_{BOS}	Input offset current	T_A = 25°C	–1	0.1	1	µA	A
$\Delta I_{BOS}/\Delta T$	Input offset current drift	T_A = –40°C to +85°C		2		nA/°C	B
CMRR	Common-mode rejection ratio	V_{CM} = ±0.5 V referred to midsupply	90	100		dB	A
INPUT							
	Common-mode input resistance			2		MΩ	C
C_{CM}	Common-mode input capacitance			0.6		pF	C
	Differential input resistance			5		kΩ	C
C_{DIFF}	Differential input capacitance			0.2		pF	C
V_{IH}	Common-mode input range (high)	CMRR > 66 dB, V_{S+} = 3.3 V	2.7	2.9		V	A
V_{IL}	Common-mode input range (low)	CMRR > 66 dB, V_{S+} = 3.3 V		1.1	1.3	V	A
V_{IH}	Common-mode input range (high)	CMRR > 66 dB	4.4	4.6		V	A
V_{IL}	Common-mode input range (low)	CMRR > 66 dB		1.1	1.3	V	A
OUTPUT							
V_{OH}	Output voltage (high)	T_A = 25°C, V_{S+} = 3.3 V	2.35	2.4		V	A
V_{OH}	Output voltage (high)	T_A = 25°C	3.95	4.1		V	A
		T_A = –40°C to +85°C		4			B
V_{OL}	Output voltage (low)	T_A = 25°C, V_{S+} = 3.3 V		1.05	1.15	V	A

(1) Current flowing into the input pin is considered negative

Electrical Characteristics (continued)

V_{S+} = 5 V, $V_{S–}$ = 0 V, G = 7 V/V, R_F = 453 Ω, noninverting configuration, input common-mode biased at midsupply, R_L = 200 Ω, output load is referenced to midsupply, and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level
V_{OL}	Output voltage (low)	T_A = 25°C		1.05	1.15	V	A
		T_A = –40°C to +85°C		1.1			B
	Linear output drive (sink and source)	R_L = 10 Ω, A_{OL} > 60 dB	65	80		mA	A
		T_A = –40°C to +85°C, R_L = 10 Ω, A_{OL} > 60 dB		74			B
I_{SC}	Output short-circuit current		85	105		mA	A
C_{LOAD}	Capacitive load drive	30% overshoot		10		pF	C
POWER SUPPLY							
V_S	Operating voltage		3.3		5.25	V	A
I_Q	Quiescent current		16	17.5	19.5	mA	A
		V_{S+} = 3.3 V	15.5	17	19		A
		V_{S+} = 5.25 V	16.5	18	20		A
		T_A = –40°C to +85°C		19.5			B
		T_A = –40°C to +125°C		20.5			B
PSRR+	Positive power-supply rejection ratio		80	90		dB	A
PSRR–	Negative power-supply rejection ratio		70	78			
POWER DOWN							
	Disable voltage threshold	Amplifier OFF below this voltage	0.7	1		V	A
	Enable voltage threshold	Amplifier ON below this voltage		1.5	1.8	V	A
	Power-down quiescent current			0.07	0.2	mA	A
	$\overline{PD}$ bias current			0.07	0.2	mA	A
	Turnon time delay	Time to V_{OUT} = 90% of final value		13		ns	C
	Turnoff time delay	Time to V_{OUT} = 10% of original value		120		ns	C

8 Parameter Measurement Information

8.1 Parameter Measurement Information

The various test setup configurations for the OPA855 are shown below

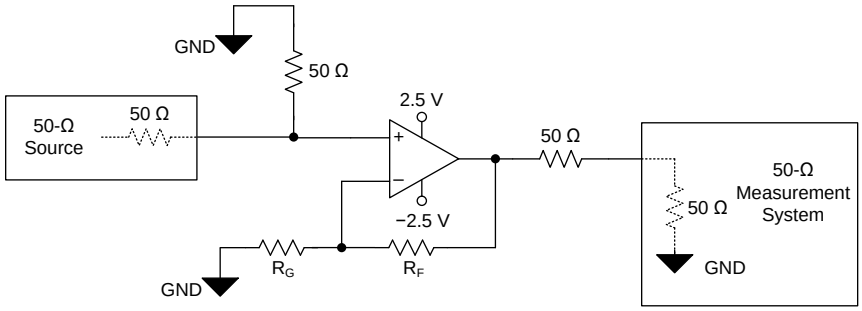

Figure 1. Noninverting Configuration

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Parameter Measurement Information (continued)

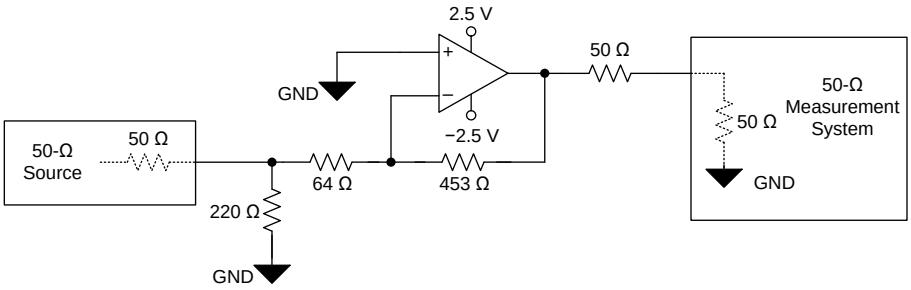

Figure 2. Inverting Configuration (Gain = –7 V/V)

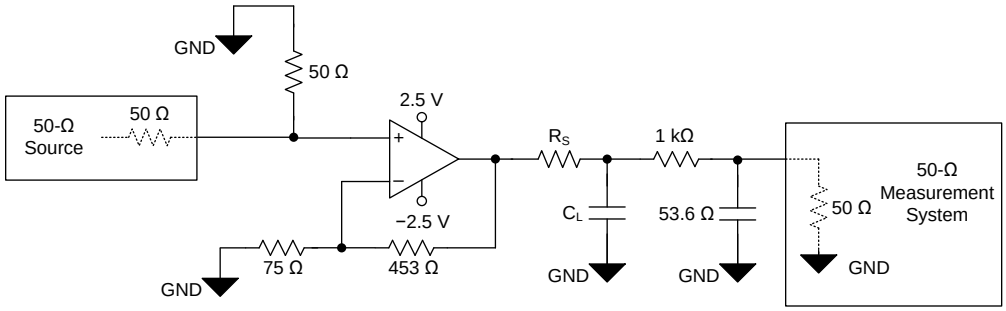

Figure 3. Capacitive Load Driver Configuration

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9 Detailed Description

9.1 Overview

The ultra-wide, 8-GHz gain bandwidth product (GBP) of the OPA855, combined with the broadband voltage noise of 0.98 nV/√Hz, produces a viable amplifier for wideband transimpedance applications, high-speed data acquisition systems, and applications with weak signal inputs that require low-noise and high-gain front ends. The OPA855 combines multiple features to optimize dynamic performance. In addition to the wide, small-signal bandwidth, the OPA855 has 850 MHz of large signal bandwidth (2 V_{PP}) and a slew rate of 2750 V/µs, making the device a viable option for high-speed pulsed applications.

The OPA855 is offered in a 2-mm × 2-mm, 8-pin, WSON package that features a feedback (FB) pin for a simple feedback network connection to the amplifier. The pinout features an isolation pin between the feedback and input connection to reduce parasitic coupling for applications that are sensitive to feedback capacitance.

9.2 Functional Block Diagram

The OPA855 is a classic, voltage feedback operational amplifier (op amp) with two high-impedance inputs and a low-impedance output. Standard application circuits are supported, like the two basic options shown in Figure 4 and Figure 5.The resistor on the noninverting pin is used for bias current cancellation to minimize the output offset voltage. In a noninverting configuration the additional resistors on the noninverting pin add noise to the system so if SNR is critical, the resistor can be eliminated. In an inverting configuration the noninverting node is typically connected to a DC voltage, so the high-frequency noise contribution from the bias cancellation resistor can be bypassed by adding a large 1-µF capacitor in parallel to the resistor to shunt the noise. The DC operating point for each configuration is level-shifted by the reference voltage (V_{REF}), which is typically set to midsupply in single-supply operation. V_{REF} is typically connected to ground in split-supply applications.

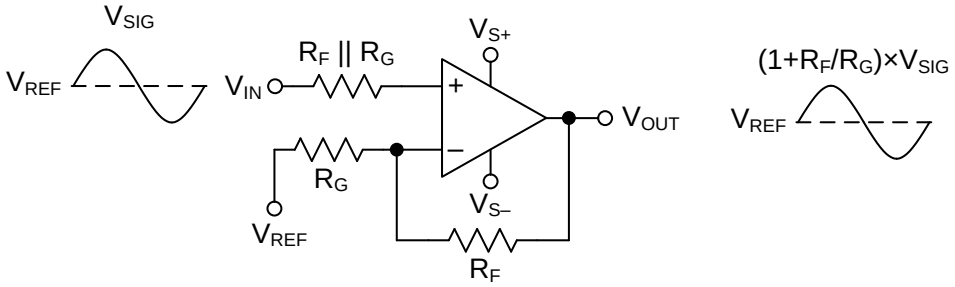

Figure 4. Noninverting Amplifier

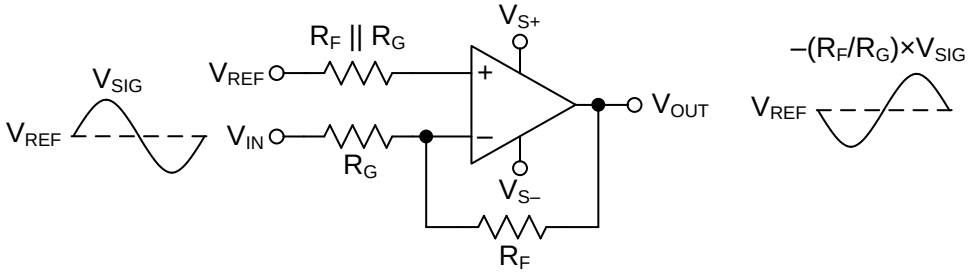

Figure 5. Inverting Amplifier

9.3 Feature Description

9.3.1 Input and ESD Protection

The OPA855 is fabricated on a low-voltage, high-speed, BiCMOS process. The internal, junction breakdown voltages are low for these small geometry devices, and as a result, all device pins are protected with internal ESD protection diodes to the power supplies as Figure 6 shows. There are two antiparallel diodes between the inputs of the amplifier that clamp the inputs during an overrange or fault condition.

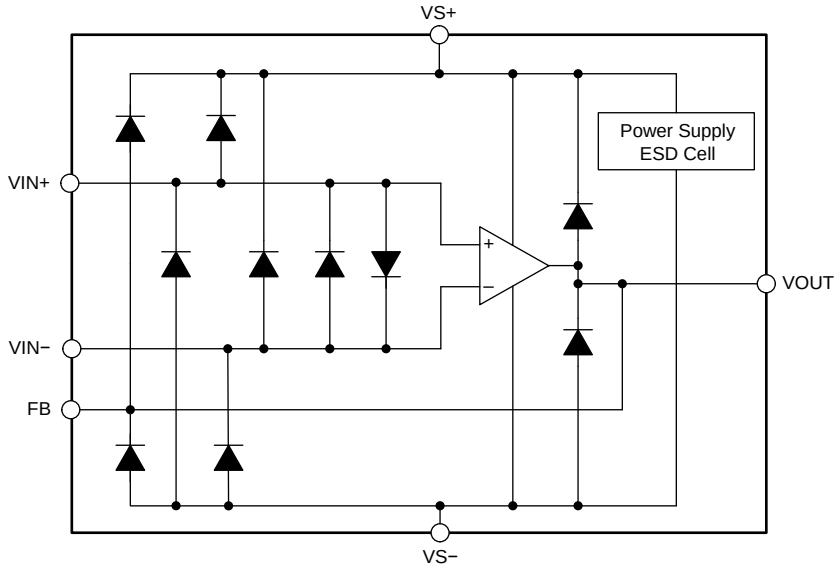

Figure 6. Internal ESD Structure

9.3.2 Feedback Pin

The OPA855 pin layout is optimized to minimize parasitic inductance and capacitance, which is critical in high-speed analog design. The FB pin (pin 1) is internally connected to the output of the amplifier. The FB pin is separated from the inverting input of the amplifier (pin 3) by a no connect (NC) pin (pin 2). The NC pin must be left floating. There are two advantages to this pin layout:

1. A feedback resistor (R_F) can connect between the FB and IN– pin on the same side of the package (see Figure 7) rather than going around the package.
2. The isolation created by the NC pin minimizes the capacitive coupling between the FB and IN– pins.

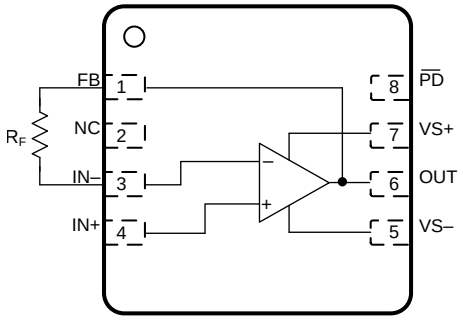

Figure 7. R_F Connection Between FB and IN– Pins

Feature Description (continued)

9.3.3 Wide Gain-Bandwidth Product

Figure 8 shows the open-loop magnitude and phase response of the OPA855. Calculate the gain bandwidth product of an op amp by determining the frequency at which the A_{OL} is 60 dB and multiplying that frequency by a factor of 1000. The second pole in the A_{OL} response occurs before the magnitude crosses 0 dB, and the resultant phase margin is less than 0°. This indicates instability at a gain of 0 dB. Amplifiers that are not unity-gain stable are known as decompensated amplifiers. Decompensated amplifiers typically have higher gain-bandwidth product, slew rate, and lower voltage noise, compared to a unity-gain stable amplifier with the same amount of quiescent power consumption.

One of the primary applications for the OPA855 is as a high-speed transimpedance amplifier (TIA), as Figure 14 shows. The low-frequency noise gain of a TIA is 1 V/V, as *What You Need To Know About Transimpedance Amplifiers – Part 1* and *What You Need To Know About Transimpedance Amplifiers – Part 2* show. The ratio of the total input capacitance and the feedback capacitance set the high-frequency gain. To maximize the TIA closed-loop bandwidth, the feedback capacitance is typically smaller than the input capacitance, which implies that the high-frequency noise gain is greater than 0 dB. As a result, op amps that are used in TIA applications are not required to be unity-gain stable, which makes a decompensated amplifier a viable option for such applications.

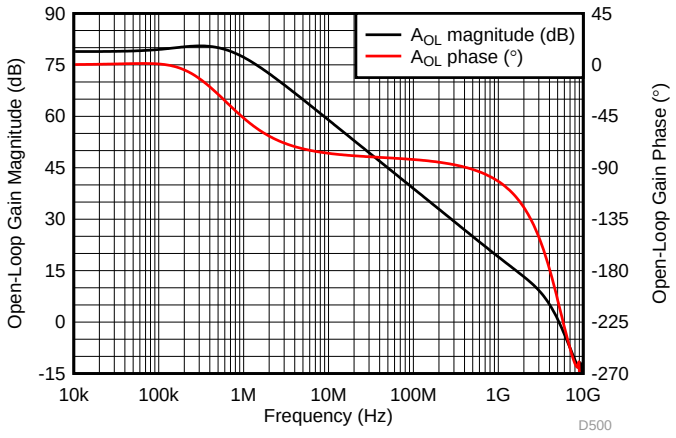

Figure 8. A_{OL} (No Load) Versus Frequency

9.3.4 Slew Rate and Output Stage

In addition to wide bandwidth, the OPA855 features a high slew rate of 2750 V/µs. The slew rate is a critical parameter in high-speed pulse applications with narrow sub 10-ns pulses such as Optical Time-Domain Reflectometry (OTDR) and LIDAR. The high slew rate of the OPA855 implies that the device accurately reproduces a 2-V, 1-ns pulse edge. The wide bandwidth and slew rate of the OPA855 are designed for high-speed, signal-chain front ends.

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Feature Description (continued)

Figure 9 shows the open-loop output impedance of the OPA855 as a function of frequency. To achieve high slew rates and low output impedance across frequency, the output swing of the OPA855 is limited to approximately 3 V. The OPA855 is typically used in conjunction with high-speed pipeline ADCs and flash ADCs that have limited input ranges. Therefore, the OPA855 output swing range coupled with the class-leading voltage noise specification for a CMOS amplifier maximizes the overall dynamic range of the signal chain.

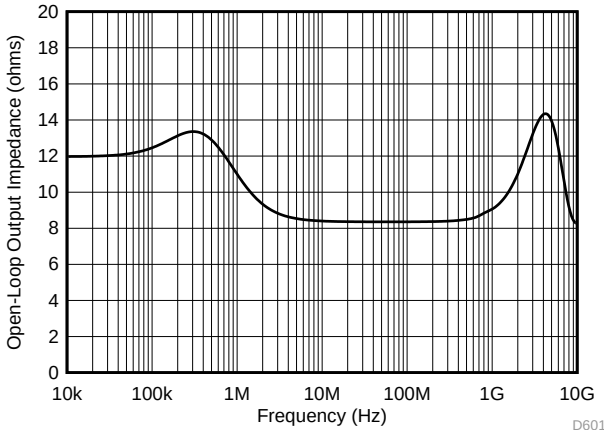

Figure 9. Open-Loop Output Impedance (Z_{OL}) Versus Frequency

9.4 Device Functional Modes

9.4.1 Split-Supply and Single-Supply Operation

The OPA855 can be configured with single-sided supplies or split-supplies. Split-supply operation using balanced supplies with the input common-mode set to ground eases lab testing because most signal generators, network analyzers, spectrum analyzers, and other lab equipment typically reference inputs and outputs to ground. Split-supply operation is preferred in systems where the signals swing around ground. However, the system requires two supply rails. In split-supply operation, the thermal pad must be connected to the negative supply.

Newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA855 can be used with a single positive supply (negative supply at ground) with no change in performance if the input common-mode and output swing are biased within the linear operation of the device. To change the circuit from a split-supply to a single-supply configuration, level shift all the voltages by half the difference between the power supply rails. In this case, the thermal pad must be connected to ground.

9.4.2 Power-Down Mode

The OPA855 features a power-down mode to reduce the quiescent current, which conserves power. Driving the $\overline{PD}$ pin LOW (less than 0.8 V) disables the amplifier, consuming a standby current of less than 200 µA. Raise the $\overline{PD}$ pin HIGH (greater than 1.2 V) to enable the amplifier.

The $\overline{PD}$ disable and enable threshold voltages are with reference to the negative supply. If the amplifier is configured with the positive supply at 3.3 V and the negative supply at ground, then the disable and enable threshold voltages are 0.8 V and 1.2 V, respectively. If the amplifier is configured with ±2.5-V supplies, then the threshold voltages are at –1.7 V and –1.3 V, respectively.

Connecting the $\overline{PD}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a noninverting amplifier, the feedback (R_F) and gain (R_G) resistor network form a parallel load to the output of the amplifier. To protect the input stage of the amplifier, the OPA855 uses internal, back-to-back protection diodes between the inverting and noninverting input pins as Figure 6 shows. When the differential voltage between the input pins of the amplifier exceeds a diode voltage drop, an additional low-impedance path is created between the inputs.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Using the OPA855 in Low Gain Configurations

The OPA855 is compensated to have less than 1 dB of peaking in a gain of 7 V/V. Using the device in lower gains results in increased peaking and potential instability. The stability of the amplifier at lower gains is increased by adding an input capacitor and a feedback capacitor to increase the high-frequency noise gain (1/β). The stability and phase margin of the amplifier depends on the loop-gain of the amplifier, which is the product of the A_{OL} and 1/β of the amplifier. If done carefully, increasing 1/β increases the loop gain which improves the phase margin. The modified network with the added capacitors alters the high-frequency noise gain, but does not alter the signal gain.

Figure 10 shows the OPA855 circuit configured in a signal gain of 7 V/V. Figure 11 shows the OPA855 circuit configured in a signal gain of 3 V/V, with a 1-pF and 0.4-pF capacitors added between the amplifier inputs and in the feedback network respectively to shape the high-frequency noise gain. *AN-1604 Decompensated Operational Amplifiers* application report provides a detailed analysis of noise gain-shaping techniques for decompensated amplifiers and shows how to choose external resistors and capacitor values.

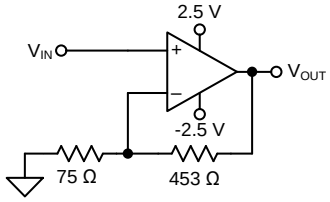

Figure 10. OPA855 Configured in a Gain of 7 V/V

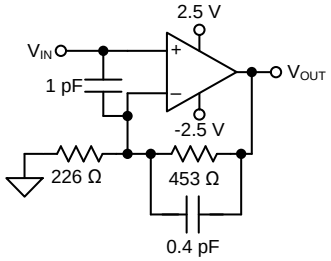

Figure 11. OPA855 Configured in a Gain of 3 V/V

Figure 12 shows the simulated frequency response. Without the added noise gain shaping components, the OPA855 shows approximately 14 dB of peaking in a gain of 3 V/V. The noise-gain shaping elements reduce the peaking to less than 0.5 dB. The 1-pF input capacitor, the input capacitance of the amplifier, and the feedback network create a zero in the noise-gain at a frequency *f*, as Equation 1 shows.

$$f = \frac{1}{2\pi(R_F \,||\, R_G)C_{IN}} \quad (1)$$

where

- R_F is the feedback resistor
- R_G is the input or gain resistor
- C_{IN} is the total input capacitance, which includes the external 1-pF capacitor, the amplifier input capacitance, and any parasitic PCB capacitance.

The noise-gain zero increases the noise gain at higher frequencies which is important when compensating a decompensated amplifier. However, the noise-gain zero reduces the loop gain phase which results in a lower phase margin. To counteract the phase reduction due to the noise-gain zero, add a pole to the noise-gain curve by inserting the 0.4-pF feedback capacitor. The pole occurs at a frequency shown in Equation 2. The noise-gain pole and zero locations must be selected so that the rate-of-closure between the magnitude curves of A_{OL} and 1/β is approximately 20 dB. To ensure this occurs, the noise-gain pole must occur before the 1/β magnitude curve intersects the A_{OL} magnitude curve. The noise-gain pole must occur before $|A_{OL}| = |1/\beta|$. The point at which the two curves intersect is called the loop gain crossover frequency.

ADVANCE INFORMATION

Application Information (continued)

$$f = \frac{1}{2\pi R_F C_F} \quad (2)$$

where

- C_F is the feedback capacitor

Adding the noise-gain shaping elements increases the total output noise. Figure 13 shows a comparison of the output noise spectrum of the three configurations. The peaking shown in the closed-loop frequency response is reflected in the output noise spectrum. The low-frequency output noise in a gain of 7 V/V is higher than the other two configurations, but that is expected since the amplifier is configured at a higher DC gain. lists a comparison of the three different configurations, assuming a 3.5-GHz brickwall filter is used. The results show that the noise-shaped gain of 3 V/V degrades the input-referred noise performance compared to the configuration with a gain of 7 V/V. However, it is possible to compensate a decompensated amplifier in a gain lower than the recommended minimum specification without stability issues. For more information on op amp stability, watch the *TI Precision Lab series on stability.* video.

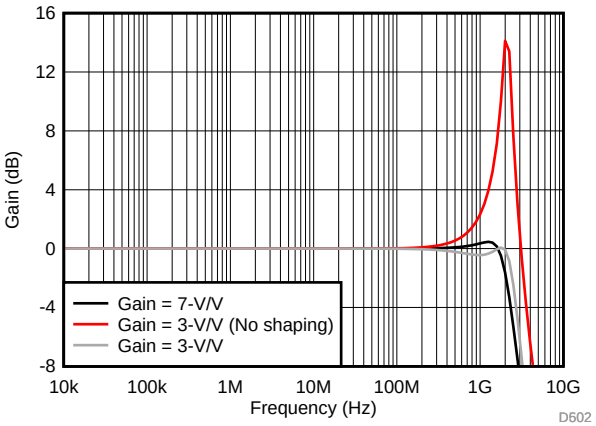

Figure 12. Normalized Frequency Response

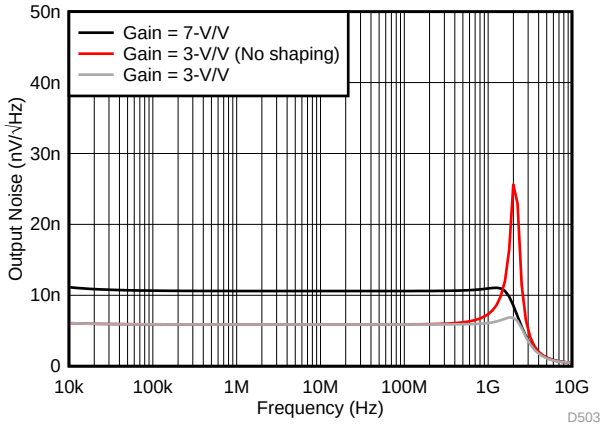

Figure 13. Output Noise Spectral Response

Table 1. OPA855 Noise Comparison

AMPLIFIER CONFIGURATION	$f_{-3\ dB}$ BANDWIDTH (GHz)	TOTAL OUTPUT INTEGRATED NOISE (3.5-GHz BANDWIDTH)	INPUT REFERRED NOISE (3.5-GHz BANDWIDTH)
Gain = 7 V/V	2.2	515 μV_{RMS}	73.5 μV_{RMS}
Gain = 3 V/V (no shaping)	3.5	711 μV_{RMS}	237 μV_{RMS}
Gain = 3 V/V	2.6	335 μV_{RMS}	111.7 μV_{RMS}

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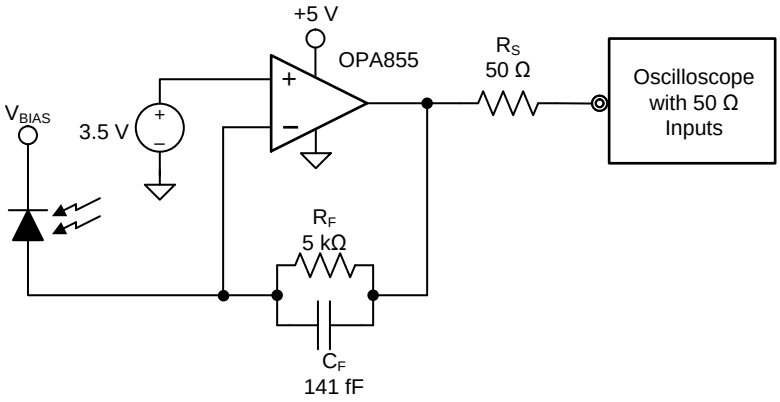
10.2 Typical Application

The high GBWP, low input voltage noise and low input capacitance of the OPA855 make the device a viable, wideband, transimpedance amplifier for low to moderate transimpedance gains. As the transimpedance gain increases the input bias current of the OPA855 coupled with the feedback resistance produces an offset voltage that reduces the available signal swing at the output. The bias current noise starts to become a significant contributor to the total noise of the system. For these reasons an op amp with bipolar inputs is not recommended for very large transimpedance gain designs.



Supply decoupling not shown

Figure 14. TIA Circuit (Gain = 5 kΩ)

10.2.1 Design Requirements

Design a high-bandwidth, transimpedance amplifier with the design requirements listed in Table 2.

Table 2. Design Requirements

TARGET BANDWIDTH (MHz)	TRANSIMPEDANCE GAIN (kΩ)	PHOTODIODE CAPACITANCE (pF)	FREQUENCY PEAKING (dB)
> 300	5	1.5	< 0.5

10.2.2 Detailed Design Procedure

The *Transimpedance Considerations for High-Speed Amplifiers* application report discusses theories and equations that show how to compensate a transimpedance amplifier for a particular transimpedance gain and input capacitance. The bandwidth and compensation equations from the application report are available in a Microsoft® Excel® calculator. A link to the calculator can be found at *What You Need To Know About Transimpedance Amplifiers – Part 1*. Set the calculator parameters as listed in Table 3.

Table 3. Inputs to the TIA Calculator

INPUT PARAMETER	INPUT VALUE	UNITS
Op Amp Gain Bandwidth Product (GBP)	8	GHz
Total Input Capacitance (C_{IN})	2.5	pF
Transimpedance Gain (R_F)	5	kΩ

The total input capacitance includes the diode capacitance (1.5 pF), an estimated PCB parasitic capacitance of 0.2 pF, the OPA855 common-mode capacitance (0.6 pF), and the differential capacitance (0.2 pF). Table 4 lists the calculated outputs.

Table 4. TIA Calculator Outputs

OUTPUT PARAMETER	OUTPUT VALUE	UNITS
Feedback capacitor (C_F)	0.141	pF
Closed-loop bandwidth	319	MHz

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The high-frequency noise gain is given by $\left(1+\frac{C_{IN}}{C_F}\right)$, and in this case, is equal to $\left(1+\frac{2.5\text{ pF}}{0.141\text{ pf}}\right)=17.7\text{ V / V}$, which is greater than the recommended gain of 7 V/V that ensures sufficient phase margin. A feedback capacitor of 0.141 pF is difficult to implement in an actual circuit because the capacitor is highly susceptible to parasitic capacitance from the PCB and the feedback resistor. Figure 15 shows the small-signal frequency response of the TIA circuit in Figure 14. The figure compares the frequency response in two cases:

- C_F = 0.141 pF
- C_F = 0.191 pF (0.05 pF larger)

With a feedback capacitance of 0.141 pF, the closed-loop bandwidth is equal to 309 MHz, which is close to the calculated value shown in Table 4. A feedback capacitance of 0.191 pF results in a closed-loop bandwidth of 202 MHz. Take care to minimize parasitic capacitance during layout. Use two 2.5-kΩ resistors in series to reduce the parasitic capacitance that is associated with the 5-kΩ feedback resistor. This results in a theoretical 50% reduction in parasitic capacitance.

The common-mode input is set to 3.5 V and the photodiode is biased to source current. This combination of amplifier common-mode and photodiode bias configuration results in a negative swing when light is incident on the photodiode which maximizes the output swing of the amplifier. In the case of the OPA855, the common-mode limit can be set as high as 4 V, which results in a 3 V_{PP} output swing. Figure 16 shows a comparison of the transient response to a 100-µA, 10-ns, input current pulse from the photodiode. The resulting amplifier output is a 0.5-V_{PP} negative pulse on a 3.5-V common-mode. Figure 17 shows a comparison of the output noise spectrum of the two cases. A 0.191-pF feedback capacitor results in lower overall noise as a result of the reduced noise gain peaking.

10.2.3 Application Curves

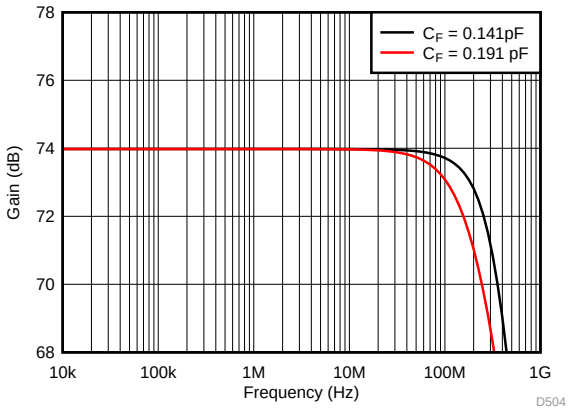
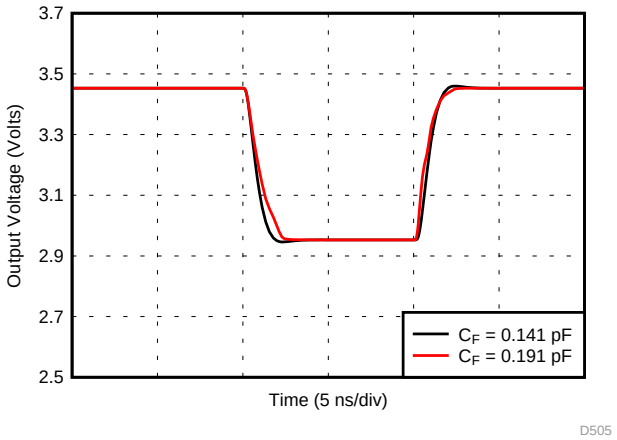


Figure 15. TIA Frequency Response



Pulse width = 10 ns Input common-mode = 3.5 V
Input = 100 μA_{PP}

Figure 16. TIA 0.5-V_{PP} Pulse Response

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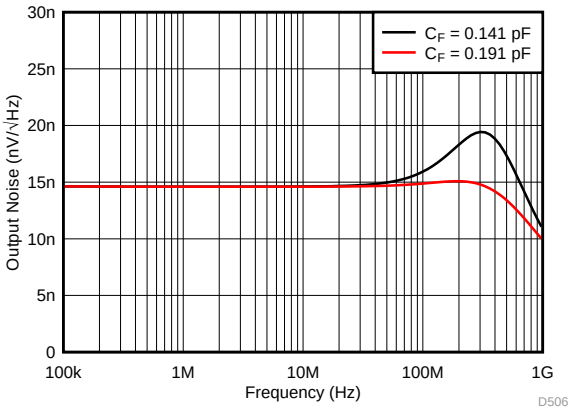


Figure 17. TIA Output Noise Spectral Response

Table 5. TIA Performance Summary

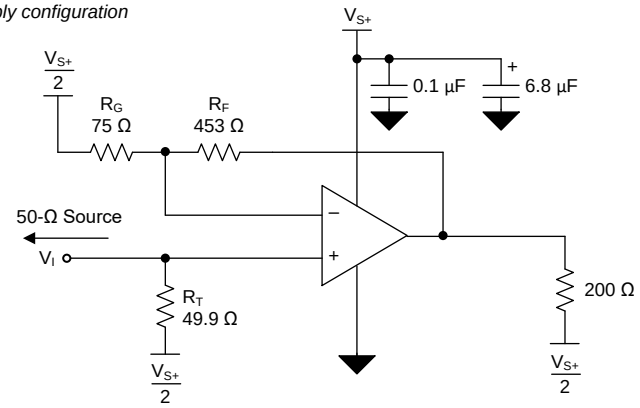
OUTPUT PARAMETER	C_F = 0.141 pF	C_F = 0.191 pF
Closed-loop bandwidth, f_{-3dB} (MHz)	309	202
Integrated input referred noise, Noise Bandwidth = 1 GHz(nA_{RMS})	102	84.2
Integrated input referred noise, Noise Bandwidth = f_{-3dB}(nA_{RMS})	60.6	42.2

ADVANCE INFORMATION

11 Power Supply Recommendations

The OPA855 operates on supplies from 3.3 V to 5.25 V. The OPA855 operates on single-sided supplies, split and balanced bipolar supplies, and unbalanced bipolar supplies. Because the OPA855 does not feature rail-to-rail inputs or outputs, the input common-mode and output swing ranges are limited at 3.3-V supplies.

a) Single supply configuration



b) Split supply configuration

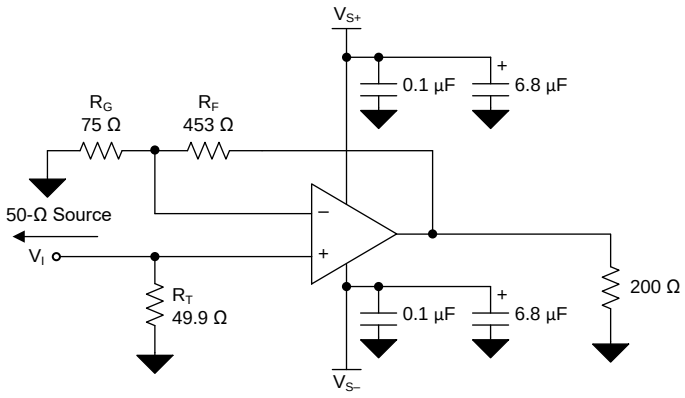


Figure 18. Split and Single Supply Circuit Configuration

ADVANCE INFORMATION

12 Layout

12.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA855 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

1. Minimize parasitic capacitance from the signal I/O pins to AC ground. Parasitic capacitance on the output and inverting input pins can cause instability. To reduce unwanted capacitance, TI recommends cutting out the power and ground traces underneath the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board. When configuring the amplifier as a TIA, if the required feedback capacitor is under 0.15 pF, consider using two series resistors, each of half the value of a single resistor in the feedback loop to minimize the parasitic capacitance from the resistor.
2. Minimize the distance (less than 0.25") from the power-supply pins to high-frequency bypass capacitors. Use high quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies to ensure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must be used on the supply pins. These are placed further from the device and are shared among several devices in the same area of the PC board.
3. **Using the OPA855 with a photodiode.** When using the OPA855 with a photodiode, ensure that the photodiode is placed as close to the inverting pin of the amplifier as possible and on the same side of the PCB as the amplifier. Excess capacitance leads to increased noise and excess inductance affects the high-frequency noise-gain response that causes instability.
4. **Careful selection and placement of external components preserves the high-frequency performance of the OPA855 .** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon-composition axially-leaded resistors provide good high-frequency performance. Keep leads and PCB trace length as short as possible. Never use wirewound resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close to the output pin as possible. Place other network components (such as noninverting input termination resistors) close to the package. Even with a low parasitic capacitance shunting the external resistors, high resistor values create significant time constants that can degrade performance. Good axial metal film or surface mount resistors have approximately 0.2 pF in shunt with the resistor. When configuring the OPA855 as a voltage amplifier, keep resistor values as low as possible and consistent with load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because R_F and R_G become part of the output load network of the amplifier.
5. **TI does not recommend socketing a high-speed device such as the OPA855.** The socket introduces additional lead length and pin-to-pin capacitance that creates a troublesome parasitic network. This can make achieving a smooth, stable, frequency response almost impossible. Solder the op amp onto the board for optimal results.

12.2 Layout Example

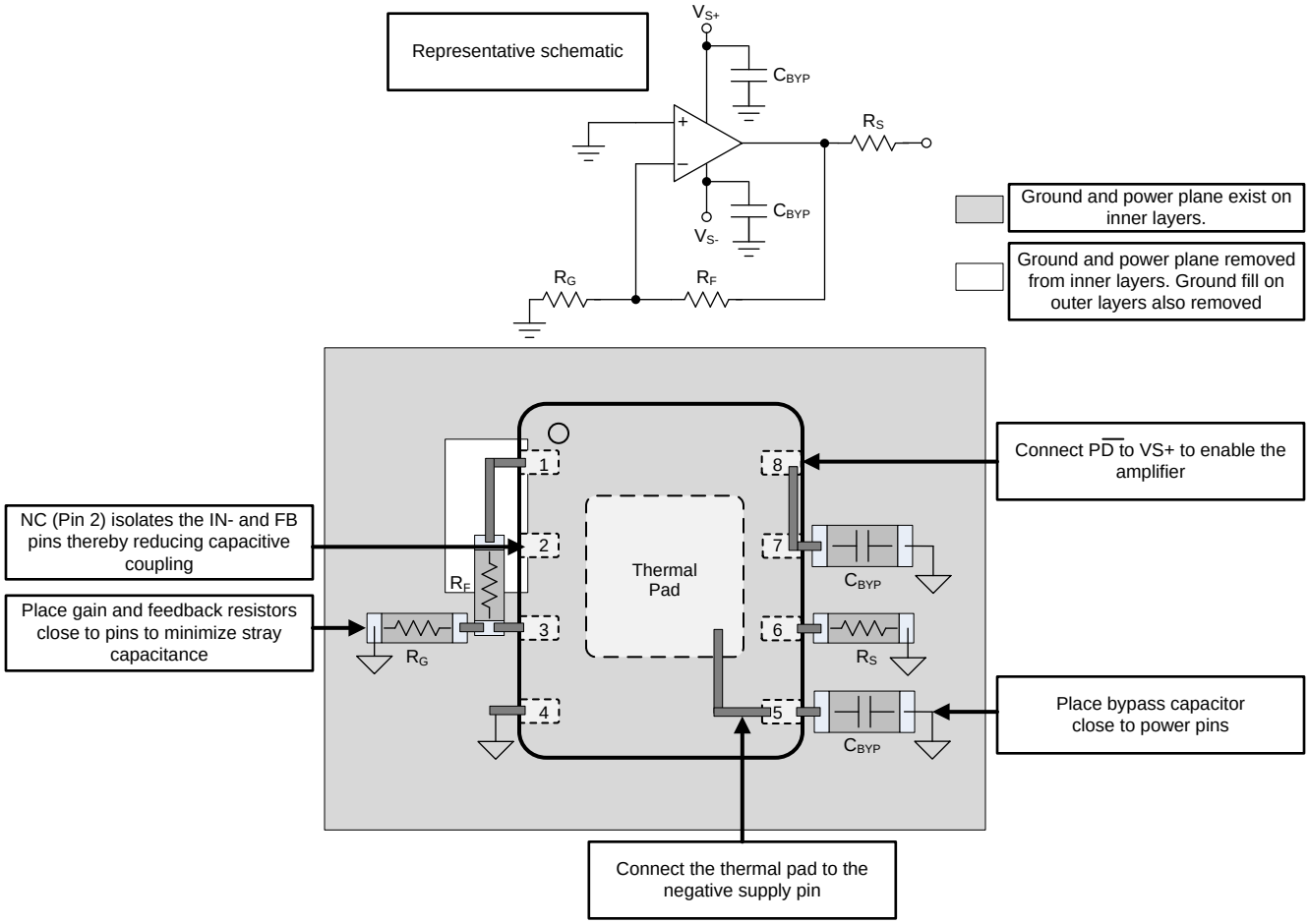


Figure 19. Layout Recommendation

When configuring the OPA855 as a transimpedance amplifier additional care must be taken to minimize the inductance between the avalanche photodiode (APD) and the amplifier. APD packaging can be quite large which often requires the APD to be placed further away from the amplifier than ideal. The added distance between the two device results in increased inductance between the APD and op amp feedback network as shown in Figure 20. The added inductance is detrimental to a decompensated amplifiers stability since it isolates the APD capacitance from the transimpedance amplifier's noise-gain equation. The noise-gain is given by Equation 3. The added PCB trace inductance between the feedback network increases the denominator in Equation 3 thereby reducing the noise-gain and the phase margin. In cases where a leaded APD in a TO can is used inductance should be further minimized by cutting the leads of the TO can to be as short as possible.

The layout shown in Figure 20 can be improved by following some of the guidelines shown in Figure 21. The two key rules to follow are:

- Add and isolation resistor R_{ISO} as close as possible to the amplifiers inverting input. Choose R_{ISO} to be between 10 Ω -20 Ω. The resistor dampens the potential resonance caused by the trace inductance and the amplifiers internal capacitance.
- Close the loop between the feedback elements (R_F and C_F) and R_{ISO} as close as possible to the APD pins. This ensures a more balanced layout and reduces the inductive isolation between the APD and the feedback network.

$$\text{Noise Gain} = \left(1 + \frac{Z_F}{Z_{IN}}\right)$$

where

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Layout Example (continued)

- Z_F is the total impedance of the feedback network.
- Z_{IN} is the total impedance of the input network. (3)

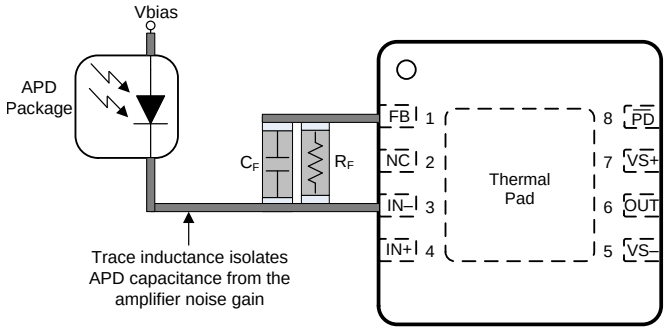

Figure 20. Non-Ideal TIA Layout

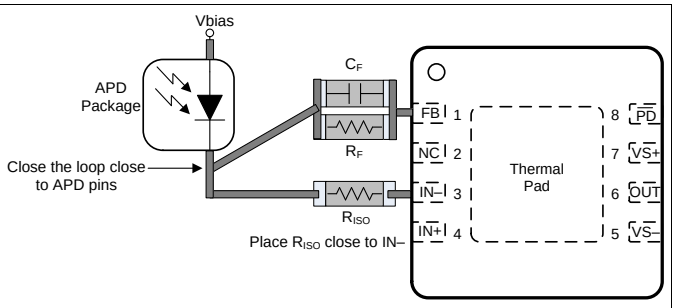

Figure 21. Improved TIA Layout

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

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13.2 Community Resources

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13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA855IDSGT	PREVIEW	WSON	DSG	8	250	TBD	Call TI	Call TI	-40 to 125		
XOPA855IDSGT	ACTIVE	WSON	DSG	8	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

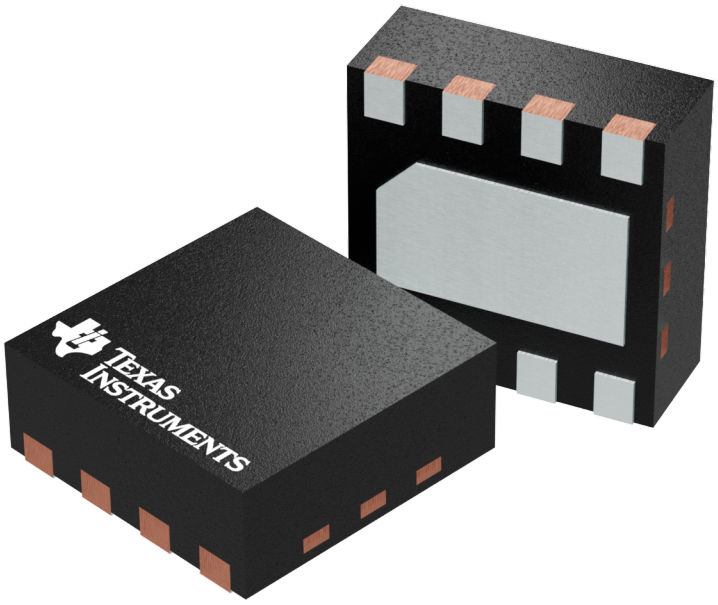
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DSG 8 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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